

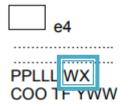
# PRODUCT/PROCESS CHANGE NOTIFICATION PCN 10803 – Additional information

## Extended STM32F listed products – TSMC Singapore Wafer Fab SSMC additional source

### **MDG** - Microcontrollers Division (MCD)

#### How can the change be seen?

The standard marking is:



**WX** code indicates the diffusion traceability plant code.

Please refer to the <u>DataSheet</u> for marking details.

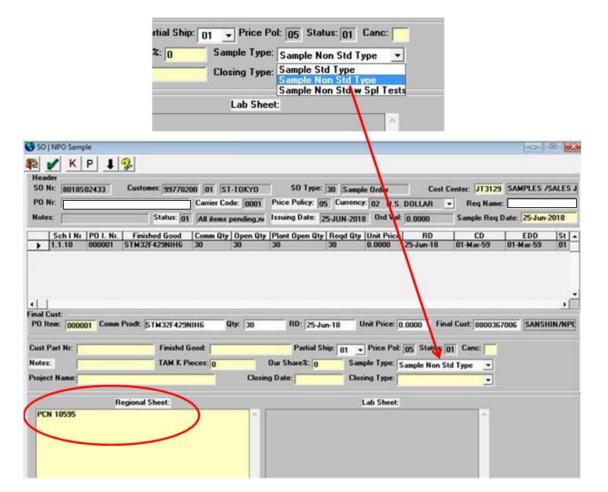
### The marking is changing as follows:

Existing		Additional		
WX code Fab		WX code	Fab	
9U	TSMC USA Wafer Fab 11	9C	TSMC Singapore Wafer Fab SSMC	
98	TSMC Taiwan Wafer Fab 8			

#### How to order samples?

For all samples request linked to this PCN, please:

- place a <u>Non-standard</u> sample order (choose Sample Non Std Type from pull down menu)
- insert the PCN number "PCN10803" into the NPO Electronic Sheet/Regional Sheet
- request sample(s) through Notice tool, indicating a single Commercial Product for each request





# RER1802 for PCN10553 & PCN10803 STM32F listed products – TSMC Singapore Wafer Fab SSMC additional source

## **Reliability Evaluation Plan**

February, 5th 2019

MDG Quality & Reliability Department



## STM32F listed products – TSMC Singapore Wafer Fab SSMC additional source STM32 Die Test Vehicles

Die Vehicle	Process Perimeter	Assembly Line	Package	Number of Reliability Lots
422	TSMC 0.18μm	ATP1	LQFP100	
440		JSCC	LQFP64	
444		MUAR	LQFP48	3 lots to qualify Process Perimeter
445		JSCC	LQFP48	Then 1 lot by Die
448		ST MUAR	LQFP100	



## STM32F listed products – TSMC Singapore Wafer Fab SSMC additional source 3 STM32 Die Reliability Trials

Reliability Trial & Standard		Test Conditions	Pass Criteria	Lot Strategy	Units per Lot
ESD HBM	ANSI/ESDA/JEDEC JS-001 JESD22-A114	25°C	2kV (class 2)	1 to 2 lots	3
LU	JESD78	125°C REG-ON Configuration 125°C REG-OFF Configuration	No concern	1 to 2 lots	6 / configuration
EDR + Bake	JESD22-A117 JESD22-A103	125°C & 3.6V Cycling 150°C Bake	10k cycles 1500h 1000h	1 to 2 lots 1 <sup>st</sup> product driver Other products	77
EDR + Bake	JESD22-A117 JESD22-A103	25°C & 3.6V Cycling 150°C Bake	10k cycles 168h	1 to 2 lots	77
EDR + Bake	JESD22-A117 JESD22-A103	-40°C & 3.6V Cycling 150°C Bake	10k cycles 168h	1 to 2 lots	77
ELFR	JESD22-A108 JESD74	125°C & 3.6V	48h	1 to 2 lots	800 units for products driver 500 units for other products
HTOL	JESD22-A108	125°C & 3.6V	1200h 600h	1 to 2 lots 1 <sup>st</sup> product driver Other products	77



# STM32F listed products – TSMC Singapore Wafer Fab SSMC additional source STM32 Package Test Vehicles

Package Line	Assembly Line	Package	Wire	Die Vehicle / Partial Rawline	Number of Reliability Lots		
LQFP	ATP1	LQFP14*14 100L	Au	422 / 1L*422			
	ST MUAR	LQFP14*14 100L	Ag	422 / 1L*422			
	ST MUAR	LQFP14*14 100L	Ag	448 / 1L*448			
	JSCC	LQFP10*10 64L	Ag	440 / 5W*440			
	JSCC	LQFP7*7 48L	Ag	445 / 5B*445			
QFN	ASEKH	LQFP7*7 48L	Au	440 / 5B*440	3 lots to qualify Process Perimeter		
	MUAR	LQFP7*7 48L	Ag	444 / 5B*444	Then 1 lot by Package Assembly Line		
	JSCC	UQFN7*7 48L	Ag	440 / MI*440			
	JSCC	UQFN4*4 28L COL	Au	444 / MB*444			
TSSOP	STS	TSSOP20 Body 4.4	dy 4.4 Ag 444 / YA*444				
UFBGA	ATP3	UFBGA64 5x5	Au	440 / 21*440			
WLCSP	SCS	WLCSP 100b	NA	422 / 1M*422			



# STM32F listed products – TSMC Singapore Wafer Fab SSMC additional source STM32 Package Reliability trials

Reliability Trial & Standard		Test Conditions	Pass Criteria	Lot Strategy	Units per Lot
PC	Pre Conditioning Moisture Sensitivity Jedec Level 1 (*) Moisture Sensitivity Jedec Level 3 (*) J-STD-020/ JESD22-A113	Bake (125°C / 24h) Soak (85°C / 85% RH / 168 hrs) for level 1 (*) Soak (30°C / 60% RH / 192h) for level 3 (*) Convection reflow: 3 passes	3 Passes	1 to 2 lots	231 to 308 (***)
UHAST (**) (***)	Unbiased Highly Accelerated Temperature & Humidity Stress JESD22-A118	130°C, 85%RH, 2 Atm	96h	1 to 2 lots	77
TC (**)	Thermal Cycling  JESD22 A104	-50°C, +150°C Or equivalent -65°C +150°C	1000Cy 500Cy	1 to 2 lots	77
THB (**) Or HAST (**)	Temperature Humidity Bias JESD22-A101 Or Biased Highly Accelerated temperature & humidity stress JESD22 A110	85°C, 85% RH, bias Or 110°C, 1.2 atm , 85% RH bias	1000h Or 264h	1 to 2 lots	77
HTSL (**)	High Temperature Storage Life JESD22-A103	150°C - no bias	1000h	1 to 2 lots	77
Construction Analysis	JESD22-B102 JESD22-B100/B108	Including Solderability & Physical Dimensions	No concern	1 by package assembly line	15 10
ESD CDM	ESD Charged Device Model ANSI/ESD STM5.3.1	Aligned with device datasheet	250V to 500V	1 by package assembly line	3



<sup>(\*)</sup> MSL1 for packages TSSOP20 and WLCSP100 MSL3 for other packages (LQFP48, LQFP64, LQFP100, UQFN28 COL, UQFN48, UFBGA64)

<sup>(\*\*)</sup> Tests performed after preconditioning

<sup>(\*\*\*)</sup> UHAST not done for BGA

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